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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,880	10/31/2003	Shigeru Yamada	OHG 139	8980
23995	7590	03/21/2006	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			NINO, ADOLFO	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/697,880

Applicant(s)

YAMADA, SHIGERU

Examiner

Adolfo Nino

Art Unit

2831

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-14, 17-22 and 24-30 is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 1, 15, 16 and 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/31/03; 9/13/04</u> . | 6) <input checked="" type="checkbox"/> Other: <u>Reasons for allowance</u> .            |

***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

The information disclosure statements (IDS) submitted on 10/31/03 and 9/13/04 are being considered by the examiner.

***Claim Objections***

Claims 1, 15, 16 and 23 are objected to because of the following informalities:

Claim 1, line 14, before "second" insert -----a-----.

Claim 15, line 5, before "wiring" insert -----first-----.

Claim 16, line 5, before "wiring" insert -----first-----.

Claim 23, line 3, either delete "and said surfaces" or make "surfaces" singular and insert ----comprising---- after it.

Claim 23, line 5, before "bump" insert -----a-----.

Appropriate correction is required.

***Allowable Subject Matter***

Claims 2-14, 17-22 and 24-30 are allowed.

Claims 1, 15, 16 and 23 would be allowable if rewritten to overcome the objections set forth in this Office action.

The following is an examiner's statement of reasons for allowance:

With respect to claims 1-22, the cited prior art do not disclose, teach or suggest, alone or in combination, the claimed semiconductor device, comprising: a semiconductor chip, a wiring layer, and a sealing layer which covers the perimeter and main surface of said semiconductor chip such that the surface of said wiring layer is exposed, wherein said wiring layer is provided in the surface of said sealing layer, and extends from a first region of said sealing layer over said main surface to a second region of said sealing layer outside the first region.

With respect to claims 23-30, the cited prior art do not disclose, teach or suggest, alone or in combination, the claimed semiconductor device, comprising: a semiconductor chip, a first wiring structure, a second wiring structure electrically connected to the first wiring structure, a sealing layer which covers the main surface and the side surfaces of the semiconductor chip, wherein the second wiring structure extends from a first region to a second region, the first region being located at the sealing layer over the main surface of the semiconductor chip and the second region being positioned at the sealing layer formed on the side surfaces of the semiconductor chip.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art disclose a semiconductor device having a semiconductor chip having an electrode pad and a wiring portion including a bump portion, but does disclose a sealing layer which covers the perimeter and main surface of said semiconductor chip such that the surface of said wiring layer is exposed, wherein said wiring layer is provided in the surface of said sealing layer, and extends from a first region of said sealing layer over said main surface to a second region of said sealing layer outside the first region, or a sealing layer which covers the main surface and the side surfaces of the semiconductor chip, wherein the second wiring structure extends from a first region to a second region, the first region being located at the sealing layer over the main surface of the semiconductor chip and the second region being positioned at the sealing layer formed on the side surfaces of the semiconductor chip: Kelkar et al. (US 6,900,532 B1); Kimura (US 6,690,090 B2); Takahashi et al. (US 6,576,984 B2); Murata et al. (US 6,525,424 B2); Kata (6,114,754); Horiuchi et al. (US 6,084,295); Sakurai (US 6,078,104); Andoh (US 6,627,988 B2); Sahara et al. (US 6,713,880 B2); and Imamura et al. (US 6,476,503 B1).

This application is in condition for allowance except for the following formal matters: Please see the above objections noted in this Office action.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

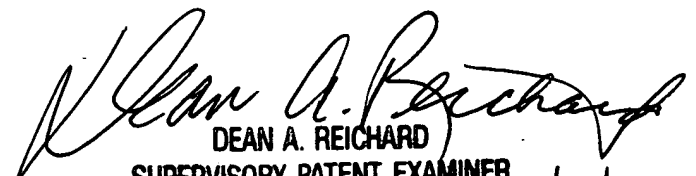
A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolfo Nino whose telephone number is (571) 272-1981. The examiner can normally be reached on M-F (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571) 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AN

  
DEAN A. REICHARD  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800 3/17/06